Remarks

Claim 23 has been amended. No claims have been canceled. Therefore, claims 1-26 are presented for examination.

In a Final Office Action mailed June 28, 2005, the Examiner has requested any documentation known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. The inventors were notified about the request and were not aware of any references qualifying as prior art. The attorney of record is also not aware of any references qualifying as prior art.

Claims 23-26 stand rejected under 35 USC § 101 for not being limited to tangible embodiments. Applicants submit that claim 23 has been amended to appear in proper condition for allowance.

Claims 1-26 stand rejected under 35 USC § 103(a) as being unpatentable over Arimilli (U.S. Patent No. 6,587,926) in view of the standard practice of integrating circuits, as further evidenced by Sherburne (U.S. Pub. No. 2002/0184546). Applicants submit that the present claims are patentable over the combination of Arimilli and Sherburne.

Arimilli discloses a system for managing a data access transaction within a hierarchical data storage system. See Arimilli at Abstract. The system includes a symmetric multiprocessor (SMP) system including a plurality of processors. Each processor includes a respective level one (L1) cache. Each processor is coupled via a processor bus to a level two cache, which are in-line caches shared by multiple processors. Each L2 cache is connected to a level three (L3) cache and to a system bus. The lower cache levels are employed to stage data to the L1 caches. L2 caches and L3

caches thus serve as intermediate storage between the processors and system memory. The L2 caches and L3 caches are connected to system memory via the system bus col. 4, ll. 8-64. Nonetheless, Arimilli does not disclose or suggest control logic to receive a first cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache.

Sherburne discloses a low power configurable processor core. See Sherburne at Abstract. However, Sherburne does not disclose or suggest control logic to receive a first cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache.

Claim 1 of the present application recites control logic coupled to first and second dedicated caches to receive a first cache line from the first dedicated cache and to transfer the first cache line to the second dedicated cache. As discussed above, neither Arimilli nor Sherburne disclose or suggest transferring a cache line from a first dedicated processor cache to control logic and to transfer the first cache line to a second dedicated processor cache from the control logic. Arimilli discloses an architecture having dedicated processor caches. However, there is no disclosure of control logic that transfers cache lines between the dedicated processor caches.

The Final Office Action performs a complex analysis of the Arimilli reference in order to conclude that Arimilli discloses transferring a cache line from a first dedicated processor cache to control logic and transfers the first cache line to a second dedicated processor cache from the control logic. See Final Office Action at pages 6 and 7. Nevertheless, applicants submit that Arimilli, at best, discloses transferring data from a first dedicated processor cache to a second processor to be processed at the second

processor upon cache misses at a second dedicated processor cache. Applicants maintain that nowhere in Aramilli is there a disclosure or suggestion of transferring cache lines from one dedicated processor cache to another dedicated processor cache.

Since neither Arimilli nor Sherburne disclose or suggest transferring a cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache, any combination of Arimilli and Sherburne would not disclose or suggest such a feature. Thus, claim 1 is patentable over Arimilli in view of Sherburne. Claims 2-11 depend from claim 1 and include additional features. Therefore, claims 2-11 are also patentable over Arimilli in view of Sherburne.

Claim 12 recites transferring a first cache line from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor and subsequently transferring the first cache line from the control logic to a second dedicated cache of the chip multi-processor. For the reasons described above with respect to clam 1, claim 12 is also patentable over Arimilli in view of Sherburne. Because claims 13-17 depend from claim 12 and include additional features, claims 13-17 are also patentable over Arimilli in view of Sherburne.

Claim 18 recites control logic coupled to first and second dedicated caches to receive a first cache line from the first dedicated cache and to transfer the first cache line to the second dedicated cache. Thus, for the reasons described above with respect to clam 1, claim 18 is also patentable over Arimilli in view of Sherburne. Since claims 19-22 depend from claim 12 and include additional features, claims 13-17 are also patentable over Arimilli in view of Sherburne.

Claim 22 recites transferring a first cache line from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor and subsequently transferring the first cache line from the control logic to a second dedicated cache of the chip multi-processor. For the reasons described above with respect to clam 1, claim 22 is also patentable over Arimilli in view of Sherburne. Because claims 23-26 depend from claim 12 and include additional features, claims 23-26 are also patentable over Arimilli in view of Sherburne.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: September 28, 2005

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980